IN THE SPECIFICATION

Please amend the Specification on page 11, by adding a new paragraph, after the third full paragraph, starting after line 23, as follows:

The synchronous memory device further includes a data buffering unit 300, a multiplexer 500 and a gio (global input/output) line driver 600, which elements are equivalent to data buffering unit 10, multiplexer 30 and line driver 40, respectively described above with reference to Figure 1.

Please amend the Abstract of the Disclosure as follows:

~~In a synchronous memory device, erroneous operation due to the ripple of the DQS signal in the write operation can be prevented.~~ A synchronous memory device, receiving a number of data in ~~synchronous~~ synchronization with a rising edge and a falling edge of a clock, includes a data strobe buffering unit, a data align latching unit and a DQS signal controlling unit. The data strobe buffering unit outputs a rising pulse and a falling pulse for detecting a rising edge and a falling edge of a DQS signal that sustains a high impedance state when there is no operation and is clocked while the data is inputted. The data align latching unit latches and aligns the data in ~~synchronous~~ synchronization with the rising pulse and the falling pulse. The DQS signal controlling unit controls the data strobe buffering unit to output the rising pulse and the falling pulse to the data align latching unit only when the DQS signal is clocked.